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APPLICATION

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**TITLE: GENERATING PULSES FOR RESETTING INTEGRATED
CIRCUITS**

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GENERATING PULSES FOR RESETTING INTEGRATED CIRCUITS

Background

This invention relates generally to integrated circuits and particularly to systems for starting up 5 integrated circuits.

During the start-up cycle of an integrated circuit, the supply voltage ramps up. A power-on reset circuit generally asserts reset whenever the supply voltage falls below a threshold. Moreover, the reset circuit asserts a 10 reset until the supply voltage has risen above the threshold for a suitable interval. The operation of the power-on reset circuit prevents various integrated circuits such as counters, phase-locked loops, filters, memories, flip-flops, and shift registers, as a few examples, from 15 operating improperly during start-up operation.

In some cases, such as those involving complex logic patterns or unexpected data patterns, an integrated circuit may be determined, incorrectly, to be in a ready state. It may be desirable to only release the circuit when it is in 20 its predetermined state. In some cases, the power-on reset circuits may release logic when the power supply has maintained its threshold level for a predetermined time even though the circuit's logic is not in its predetermined state. Conversely, the power-on reset circuit may

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improperly release the integrated circuit because the logic is in the predetermined state even though the power supply level is still ramping.

Thus, there is a need for a system that does not
5 prematurely release an integrated circuit.

Brief Description of the Drawings

Figure 1 is a block diagram of one embodiment of the present invention;

10 Figure 2 is a block diagram of one embodiment of the present invention;

Figures 3a through 3c are timing diagrams for a plurality of signals in accordance with one hypothetical embodiment;

15 Figures 4a through 4c are timing diagrams for signals in accordance with another hypothetical embodiment;

Figure 5 is a block diagram for a chip for generating a power-on reset pulse in accordance with one embodiment of the present invention;

20 Figure 6 is a circuit diagram for one of the blocks shown in Figure 5 in accordance with one embodiment of the present invention; and

Figure 7 is a circuit diagram for additional blocks in the block diagram shown in Figure 5 in accordance with one 25 embodiment of the present invention.

Detailed Description

Referring to Figure 1, a functional block F may be controlled by a power-on reset circuit 10 to prevent its release for normal operation prior to the time that both
5 the power supply has stabilized and the logic in the functional block F has transitioned to predetermined logic states. The power-on reset circuit 10, in one embodiment, may include the decision logic 12, a latch 14, a pulse generator 16, and an amplifier 18a that couples a signal feedback 20 back to the functional block F. The circuit 10
10 may be integrated on the same chip as the block F in one embodiment.

The functional block F may generate a plurality of output signals I_0 through I_N . Each of the signals is
15 received by the decision logic 12 so that the decision logic 12 can determine whether the logic of the functional block F is in the proper predetermined, initial states to begin normal operation.

During start-up, the signals I_0 through I_N may be in
20 some random state where it is highly probable that at least some of these signals are high and some are low. The decision logic 12 yields a low output to the S node of the latch 14 if one or more of the outputs I_0 to I_N of the functional block F is not in its predetermined state. The
25 decision logic tests the signals I_0 to I_N to determine whether those signals are in their proper initial states.

Meanwhile, the pulse generator 16 initially generates a high pulse into the R node of the latch 14 when the supply voltage is ramping up. The combination of a low S node and high R node may result in a reset signal being sent to the functional block F through the amplifier 18a and the signal feedback 20. Thus, the pulse generator 16 may trigger the latch 14 to generate the reset signal to place the logic in the functional block into correct initial states.

The reset signal resets the logic in the functional block F to a desired predetermined state. As a result, the outputs I_0 through I_N yield known good states. When these good states are detected by the decision logic 12, this results in the latch 14 node S going high. The reset signal remains active until the node S has become high, indicating that the functional block's logic is ready, and the pulse generator 16 signal has gone away, indicating that the power supply is now fully operational.

When the pulse generator 16 signal is gone and logic indicates ready (S node = 1), normal chip operation begins in the functional block F. If the logic in the functional block F is not ready, for example due to long routing or for some other reason, the reset remains active, preventing normal operation of the function block F.

After the logic in the functional block F is released, the decision logic 12 may indicate a faulty ready state.

This may be the result of complex logic patterns or unexpected data patterns, as two examples. The reset signal is not improvidently activated since it is latched into a deactive state by the latch 14 until the power 5 cycles. The latch 14 releases from its deactivated state (no reset) only if the pulse generator 16 indicates that the power supply is ramping.

Referring, next to Figure 2, the functional block F in this example is a counter having logic in the form of a 10 plurality of flops only a few of which are shown. The reset signal (on feedback 20) to the flops is generated as soon as the pulse generator 16 is activated. The reset signal is active regardless of the indication from the logic within the functional block F. This is a desirable 15 property because during start-up it is possible to have faulty indicators from the functional block F.

The feedback signal 20 resets the counter to a predetermined state. The counter sends an "all high" signal to the AND gate 12a (which acts as the decision 20 logic) once all the flops are in their required logic states. Once the pulse generator 16 signal is gone ($R=0$), and the counter has indicated ready ($S=1$) the reset signal goes away. When the S and R inputs are zero or the R signal is one, the reset signal is active.

Potentially, the output of the AND gate 12a may be switched between low and high levels due to normal logic 25

operation of the counter which accidentally happens to instantaneously yield the correct initial, all high condition. However, the latch 14a will not reactivate because it has been latched to its deactive (no reset) state.

Referring to Figures 3a through 3c, the power supply signal Vcc shown in Figure 3a ramps up at 22 (when turned on) to a Vcc level 24. During the ramping (at 22), as shown in Figure 3b, the pulse generator 16 signal undergoes the transition to the high level 26 causing the functional block logic to go to "ready" (S=1), as indicated at 30 in Figure 3c. When the pulse generator 16 signal is high (Figure 3b) the logic AND is high (Figure 3c), the pulse generator 16 signal goes low (R=0) as indicated at 28 in Figure 3b. The pulse generator 16 signal being low causes the reset signal to go low releasing the logic in the functional block F, as indicated at 32 in Figure 3c. Logic glitches, indicated at 34 and 36, do not reactivate the reset signal, in one embodiment of the present invention, due to the latching action.

In the event that the I_0 through I_N AND signals indicate a high prior to the pulse generator 16 signal high 26, as indicated in Figures 4b and 4c, the circuit 10 still functions correctly in one embodiment. For example, as shown in Figure 4a, during the ramp indicated at 22, the pulse generator 16 signal goes high as indicated at 26 in

Figure 4b. Since the pulse generator 16 signal is high and the logic AND is high, the pulse generator 16 signal goes low as indicated at 28. The reset low results, causing the logic to release. Again logic glitches indicated at 34 and

5 36 do not reactivate the reset signal.

The use of the latch 14 may be advantageous in some embodiments since it is useful for noise protection in low voltage applications. Noise on the supply or noise coupled from other lines may cause bouncing on critical nodes.

10 This bouncing may trigger the next stage to unexpectedly change state.

The functional blocks may be comprised of dynamic or static logic. In addition, the functional block may be a phase-locked loop (PLL). By allowing dynamic logic, the
15 state of the blocks that are used for normal operation may be monitored. Once they operate normally (reset is gone), they do not retrigger the reset pulse because of the latching operation.

Referring to Figure 5, in accordance with one
20 embodiment of the present invention, a particular pulse generator 16 is described. However, the present invention is in no way limited to the particular design depicted in Figure 5. A variety of pulse generator 16 designs may be utilized in the embodiments shown in Figures 1 and 2.

25 The pulse generator 16 shown in Figure 5 includes activation circuits 40 that handle the feedback of the

output pulse from pulse generator 16 along the line 55. In particular, the activation circuits 40 receive the feedback of the output pulse so that, once the pulse generator 16 signal goes away, the pulse generator 16 is not

- 5 inadvertently reactivated. The activation circuits 40 may also ensure that a predetermined supply voltage level is achieved before beginning the power-on reset pulse generator 16 operation in one embodiment.

The activation circuits 40 provide outputs 53a and 53b
10 to the capacitor circuits 44. A variety of known capacitor circuits 44 may be utilized in some embodiments of the present invention. One capacitor circuit 44, shown in Figure 6, receives the supply voltage Vcc at the node 53a through the capacitor 56. The Vcc-connected capacitor 56
15 is pulled to Vcc. A capacitor 64, coupled to Vss (or ground), remains at ground initially.

The capacitor 56 slowly discharges to ground through the transistor 58 that acts as a current source.

Meanwhile, the capacitor 64 begins to charge up to Vcc
20 through the low current transistor 60 and the pass gate transistor 62. Therefore, the capacitor circuits 44 count on the current to charge up or down each capacitor 56 or 64 above the trip point of the ensuing hysteresis sense stages 48. In addition, the capacitor 64, charging towards Vcc,
25 depends on the capacitor 56 that is charging to ground

before the capacitor 64 begins charging through the pass gate transistor 62.

After the supply voltage has reached its designated output level for the desired time period, the output 47a is 5 high and the output 47b is low in one embodiment. These signals are conveyed to the hysteresis sense stages 48a and 48b. The output of the hysteresis sense stage 48a may be coupled to a logic functionality 52.

The logic functionality 52 determines whether the 10 signal is at an appropriate level to accurately trigger the logic in the functional blocks being initialized. While a variety of different techniques may be utilized for testing the output of one or more hysteresis sense stages 48, in one embodiment, the most difficult logic to trigger may be 15 emulated in the logic functionality 52. In some embodiments, the toughest logic is an inverter-like stage with stacked p-channel transistors because such a stage has particularly poor headroom.

If the power supply voltage level is too low, the 20 decision logic 54 yields a pulse that may be applied as indicated in Figure 1 for example. The decision logic 54 receives signals from the hysteresis sense stages 48a and 48b. The decision logic 54 generates a high pulse if the ground connected capacitor 64 did not charge up to Vcc or 25 the power connected capacitor 56 did not charge up to Vss or the functional logic 52 did not pass the signal. The

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pulse generator 16 continues during the power supply ramp up. When that ramp up is over for a sufficient period of time, the decision logic 54 causes the pulse generator 16 output to go away.

- 5 Figures 7 and 8 show activation circuits 40 in accordance with one embodiment. The activation circuit 40a receives the feedback signal 55a. In the case where the output pulse is low, meaning that the pulse generator 16 pulse has gone away because the desired power supply
10 conditions have been met, the inverter 64a inverts the low input signal 55a to a high output on the gate of the N-channel transistor 66a. This enables the transistor 66a to conduct. If the supply voltage (Vcc) is sufficient, the transistors 66a and 70a conduct.
- 15 Thus, the activation circuit 40a, in one embodiment, is not triggered until the supply voltage has reached a level sufficient to activate both transistors 66a and 70a. At this point the supply voltage should have reached a voltage level greater than two N-channel transistor
20 threshold voltages or in one embodiment approximately 1.4 volts.

When the activation circuit 40a turns on, it shorts the capacitor node 53a in the ensuing capacitor circuit 44. In particular, the node 53a is pulled harder towards
25 ground. This pulls the output 47b harder towards ground and tends to latch the pulse generator 16 in its deactivated

state. In one embodiment, the transistor 70a may be stronger than the transistor 58.

Likewise, the circuit 40b, shown in Figure 8, receives the low input 55b and provides it to the gate of a P-channel transistor 66b. The P-channel transistor 66b turns on and turns on the transistor 70b when the threshold voltages of the transistors 66b and 70b are exceeded. When this happens, the transistor 70b decouples the capacitor 64 from the rest of the circuit and effectively latches a high output 47a through the node 53b.

Thus, the circuits shown in Figures 7 and 8 tend to latch the capacitor circuits 44 (shown in Figure 6) into their deactivated states (indicating that the output pulse is no longer needed). In particular, the circuits 40 make it harder to retrigger the pulse generator 16 prior to a power cycle.

Latching the critical nodes 53 from one threshold voltage above V_{ss} to V_{ss} may increase noise immunity in some embodiments. This may be useful, for example, for noise protection in low voltage applications, such as .7 volt applications. When the supply capacitor 56 is connected through a diode connected transistor 58 to ground, noise on the voltage supply (V_{cc}) can cause the diode node 53a to bounce. This bouncing can trigger a stage 48. The likelihood of this occurring may be reduced by using the latching operation in one embodiment.

Likewise, the capacitors 56 and 64 may be switched to the supply voltage and may be used as decoupling capacitors on the voltage supply in one embodiment. This decoupling may reduce supply noise. In addition, without the feedback 5 55, current may pass through the diode/capacitor 56 combination in the circuit 44. This current may increase the power consumption under supply noise. By shorting the diode connected transistor 58, this power consumption may be reduced.

10 The use of two threshold voltage activation circuits 40 may, in some embodiments, make it less likely that the latching starts prior to the time when the logic is operational (one threshold voltage). In addition, the charging capacitors 56 and 64 are typically used for the 15 power-on reset application only. In the embodiment shown in Figures 5 through 8, the capacitors 56 and 64 may also be used for supply decoupling. Therefore, the same component may be utilized for two different purposes, reducing layout overhead, in some embodiments.

20 While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall 25 within the true spirit and scope of this present invention.

What is claimed is: